

What is claimed:

1. A nonvolatile memory cell comprising:
 - a semiconductor substrate;
 - a vertical MOS transistor formed by alternating N-type and P-type doped layers in said
 - 5 substrate intersecting a well etched into said substrate, said well having a floating gate of
 - conductive material formed therein and insulated from and overlying said alternating N-type
 - and P-type materials by a layer of gate insulating material;
 - a word line contact comprising a layer of conductive material formed on said substrate
 - so as to extend down into said well and overlie said floating gate but insulated therefrom by
 - 10 an insulation layer; and
 - a bit line contact comprising a layer of conductive material formed on said substrate
 - so as to be in electrical contact with the drain region of said vertical MOS transistor formed in
 - said substrate.
2. A nonvolatile memory cell, comprising:
 - 15 a semiconductor substrate of a first conductivity type having a surface;
 - a buried layer in said semiconductor substrate doped so as to have a second
 - conductivity type suitable to act as a channel region of a vertical MOS transistor formed in
 - said substrate;
 - a first region of said semiconductor substrate between said buried layer and said
 - 20 surface of said substrate, and a second region of said semiconductor substrate below said
 - buried layer, both said first and second regions being doped so as to have a first conductivity
 - type;
 - a first layer of insulating material covering said surface of said substrate;
 - a recessed gate window in the form of a well etched in said semiconductor substrate
 - 25 through said first layer of insulating material, said well being deep enough to penetrate said
 - buried layer such that the side walls of said recessed gate window intersect said buried layer
 - and said first and second regions of said semiconductor substrate;
 - a second insulating layer covering the bottom of said well;
 - a gate insulating layer formed on the sidewall of said well;
 - 30 a floating gate comprising a conductive material formed on said gate insulating layer
 - with an insulating layer formed over said conductive material so as to electrically isolate said
 - floating gate from all surrounding structures, said floating gate having a dimension suitable so
 - as to overlie at least said intersection of said well with said buried layer;
 - a word line comprising conductive material deposited on said first insulating layer so
 - 35 as to extend into said well far enough to overlie at least a portion of said floating gate; and
 - a second layer of insulating material formed over said word line; and
 - a bit line formed over said surface of said semiconductor substrate but insulated from

said word line by said second layer of insulating material, and deposited in a contact window formed in said first insulating layer so as to be in electrical contact with said first region, said first region acting as a drain of said vertical MOS transistor.